FORM PTO-1390 (Modified) (REV 11-2000) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR
XA-9484	09/868331

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP98/05921	25 December 1998	

TITLE OF INVENTION
MOBILE COMMUNICATION UNIT

APPLICANT(S) FOR DO/EO/US
Yoshikuni MATSUNAGA, Isao YOSHIDA, Mineo KATSUEDA, Masatoshi MORIKAWA, and Toru Fujioka

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include itens (5), (6), (9) and (24) indicated below.
4. ☒ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☒ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
10. ☒ An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).
11. ☐ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☒ A copy of the International Search Report (PCT/ISA/210).

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☒ A change of power of attorney and/or address letter.
19. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
20. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
21. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
22. ☐ Certificate of Mailing by Express Mail
23. ☒ Other items or information:

Copy of PCT/IB/308
Change of Correspondence Address

ASSIGNEE INFORMATION
Assignee: Hitachi, Ltd.

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/868331	PCT/JP98/05921	XA-9484

24. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☐	Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO	$1000.00
☒	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO	$860.00
☐	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO	$710.00
☐	International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4)	$690.00
☐	International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4)	$100.00

ENTER APPROPRIATE BASIC FEE AMOUNT =	**$860.00**	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).	**$0.00**	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	15 - 20 =	0	x $18.00	**$0.00**	
Independent claims	1 - 3 =	0	x $80.00	**$0.00**	
Multiple Dependent Claims **(check if applicable)**.			☐	**$0.00**	
TOTAL OF ABOVE CALCULATIONS =				**$860.00**	
☐ Applicant claims small entity status. (See 37 CFR 1.27). The fees indicated above are reduced by 1/2.				**$0.00**	
SUBTOTAL =				**$860.00**	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +				**$0.00**	
TOTAL NATIONAL FEE =				**$860.00**	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).** ☒				**$40.00**	
TOTAL FEES ENCLOSED =				**$900.00**	
				Amount to be: refunded	$
				charged	$

a. ☒ A check in the amount of **$900.00** to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **50-1165** A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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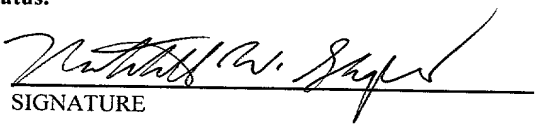


SIGNATURE

Mitchell W. Shapiro
NAME

31,568
REGISTRATION NUMBER

June 18, 2001
DATE

XA-9484

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Yoshikuni MATSUNAGA et al.

Intl. Appln. No.: PCT/JP98/05921

Intl. Filing Date: 25 December 1998

For: MOBILE COMMUNICATION UNIT

* * *

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination, please amend the above-identified patent application as indicated below.

IN THE CLAIMS;

6. (Amended) A mobile communication apparatus according to claim 1, wherein said amplifying element comprises an insulated-gate field-effect transistor.

7. (Amended) A mobile communication apparatus according to claim 1, wherein said amplifying element comprises insulated-gate field-effect transistors connected in parallel.

Please add the following claims:

8. (New) A mobile communication apparatus according to claim 2, wherein said amplifying element comprises an insulated-gate field-effect transistor.

9. (New) A mobile communication apparatus according to claim 3, wherein said amplifying element comprises an insulated-gate field-effect transistor.

10. (New) A mobile communication apparatus according to claim 4, wherein said amplifying element comprises an insulated-gate field-effect transistor.

11. (New) A mobile communication apparatus according to claim 5, wherein said amplifying element comprises an insulated-gate field-effect transistor.

12. (New) A mobile communication apparatus according to claim 2, wherein said amplifying element comprises insulated-gate field-effect transistors connected in parallel.

13. (New) A mobile communication apparatus according to claim 3, wherein said amplifying element comprises insulated-gate field-effect transistors connected in parallel.

14. (New) A mobile communication apparatus according to claim 4, wherein said amplifying element comprises insulated-gate field-effect transistors connected in parallel.

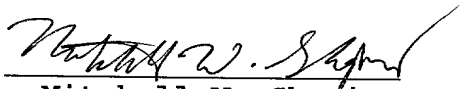
15. (New) A mobile communication apparatus according to claim 5, wherein said amplifying element comprises insulated-gate field-effect transistors connected in parallel.

REMARKS

This Preliminary Amendment eliminates the multiple dependencies from Claims 6 and 7 in order to avoid the multiple dependent claims surcharge. Claims 8-15 presented herein correspond to the dependencies eliminated from Claims 6 and 7.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

By: 
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June 18, 2001

(amended)

6. A mobile communication apparatus according to [any of] claim 1 [through claim 5], wherein said amplifying element comprises an insulated-gate field-effect transistor.

(amended)

7. A mobile communication apparatus according to [any of] claim 1 [through claim 5], wherein said amplifying element comprises insulated-gate field-effect transistors connected in parallel.

DESCRIPTION

MOBILE COMMUNICATION UNIT

Technical Field:

The present invention relates to a mobile communication apparatus which uses a microwave band of 300 MHz or above, and particularly to a technique useful for a high-frequency (RF) power amplifier which implements power amplification of RF signals.

Background Art:

In recent years, mobile communication apparatus represented by portable telephone sets based on the GSM (Global System for Mobile Communication) or PDC (Personal Digital Cellular) scheme are becoming prevalent quickly. These mobile communication apparatus are generally made up of an antenna which transmits and receives radio waves, an RF power amplifier which amplifies a power-modulated RF signal and feeds the amplified signal to the antenna, a receiver section which processes an RF signal received by the antenna, a control section which controls these functional sections, and a battery which supplies a power voltage to these functional sections. The arrangement of such mobile communication apparatus is disclosed, for example, in publication "Hitachi Review", Vol.78, No.11, pp.21-26 (published in Nov.1996).

The reason for the prevalence of mobile communication apparatus resides in the feasibility of information communication "at any time in any place with any person" owing to their features of compactness and light weight. However, in order for mobile communication apparatus to prevail further, they are required to be much smaller in size, weight and power consumption. Therefore, it is necessary to accomplish the further reduction in size, weight and power consumption of component parts of mobile communication apparatus.

One of component parts is the RF power amplifier which feeds the RF signal to the antenna. This RF power amplifier has the largest power consumption among the component parts of mobile communication apparatus. Accordingly, for the further reduction of power consumption of mobile communication apparatus, it is effective to reduce the power consumption of the RF power amplifier, i.e., improve the efficiency of the RF power amplifier. RF power amplifiers of this sort are disclosed, for example, in Japanese Patent Unexamined Publications Nos. Hei 5(1993)-152976 and Hei 8(1996)-222973.

Fig.13 is a diagram showing in brief the arrangement of an RF power amplifier which has been studied prior to the present invention. In Fig.13, reference symbol 1 denotes an input matching circuit (IMC), 2 is an inter-stage matching circuit (ISMC), 3 is an output matching circuit, 4 is a drive circuit, Pin is the input power (terminal), Vapc is the output power

control voltage, Vdd is the power voltage, and Pout is the output power (terminal). An amplifying element T1 is supplied on its gate with a bias voltage which is produced by dividing the output power control voltage Vapc with resistors R1 and R2. The amplifying element T1 is also supplied on its drain with the power voltage Vdd through a strip line SL1. The output matching circuit 3 is formed of fixed capacitors C1, C2, C3 and C4 and a strip line SL2. The capacitor C4 is a coupling capacitor for blocking a d.c. bias current. The capacitors C1-C3 have their values of capacitance and the strip line SL2 has its value of width adjusted such that the amplifying element T1 is rendered the impedance matching with the output terminal. Similarly, the input matching circuit 1 and inter-stage matching circuit 2 are each formed of multiple capacitors and a strip line so as to take impedance matching between the input terminal and the drive circuit 4 and between the drive circuit 4 and the amplifying element T1. The following explanation is based on a design example in which the signal frequency is 900 MHz and the capacitors C1-C4 are of 6 or 8 pF,7 pF,1 pF and 18 pF, respectively.

Fig.14 shows an example of the operational characteristics of the above-mentioned RF power amplifier studied prior to the present invention. Fig.14 shows by graph (A) the relation between the output power Pout and the efficiency η of the amplifier operating at the usual power

voltage Vdd of 3.5 V. The figure shows by graph (B) the relation between the power voltage Vdd and the output power Pout. The output matching circuit of this RF power amplifier implements tuning (matching) so that even if the power voltage Vdd falls to 3.0 V due to used-up power of the battery, the amplifier delivers the output power Pout of the target performance (e.g., the target performance at a signal frequency of 900 MHz is to release 3.0 W at a power voltage Vdd of 3.0 V, and release 3.6 W at 3.5 V). Namely, tuning makes much account of the output. Tuning of output priority is to have a larger output power Pout based on smaller capacitance values of the capacitors of the output matching circuit 3. With the capacitor C1 having the smaller capacitance of 6 pF, the output power Pout at a power voltage Vdd of 3.0 V is 3 W (point P11) of the target performance.

By the tuning of output priority, the output power Pout at the usual power voltage Vdd of 3.5 V becomes 4 W (point P1) as shown by graph (B) of Fig.14, which exceeds 3.6 W of the target performance. On the other hand, the efficiency η is as low as 45% (point P1) as shown by graph (A).

For the enhancement of efficiency of the RF power amplifier arranged as shown in Fig.13, only means is to alter the tuning state of the output matching circuit 3. On this account, tuning of efficiency priority is attempted. Tuning of efficiency priority is to have a higher efficiency η based on larger capacitance values of the output matching circuit 3.

Specifically, with the capacitor C1 having the larger capacitance of 8 pF, tuning is implemented to raise the efficiency η to 49% (point P2) as shown by graph (A) of Fig.14.

Implementing the tuning of efficiency priority causes the output power Pout at a power voltage Vdd of 3.5 V to become 3.6 W (point P2) of the target performance. However, if the power voltage Vdd falls to 3.0 V, the output power Pout decreases to 2.7 W (point P21) as shown by graph (B) of Fig.14, which is short of the target performance.

As described above, the RF power amplifier which has been studied prior to the present invention needs to implement tuning of efficiency priority for retaining the output power at the lower power voltage of 3.0 V in order to achieve the target performance. In consequence, it is problematic in that the efficiency is degraded, while the output power is in excess of the nominal value, at the higher power voltage of 3.5 V.

Another problem is that when tuning of efficiency priority is implemented in order to enhance the efficiency, the output power falls and is short of the target performance at the lower power voltage of 3.0 V.

The present invention is intended to solve the foregoing problems, and its object is to provide a technique of reducing the power consumption, i.e., raising the efficiency, of the RF power amplifier of mobile communication apparatus.

Another object of the present invention is to provide a

technique of further reducing the size and weight of mobile communication apparatus.

These and other objects and features of the present invention will become apparent from the following description of specification and from the accompanying drawings.

Disclosure of the Invention:

In order to achieve the above objectives, the mobile communication apparatus of this invention comprises an antenna which transmits and receives radio waves, an RF power amplifier which amplifies a power-modulated RF signal and feeds the amplified signal to the antenna, a receiver section which processes an RF signal received by the antenna, a control section which controls these functional sections, and a battery which supplies a power voltage to these functional sections, and the RF power amplifier is made up of amplifying elements of multiple stages (including a drive circuit) which amplify the RF signal, an input matching circuit which implements impedance matching for the input, an inter-stage matching circuit which implements impedance matching between the amplifying elements, and an output matching circuit which has means of varying the state of impedance matching of the output depending on the level of the power voltage which is applied to the amplifying elements.

The means of varying the state of impedance matching of

the output depending on the level of the power voltage applied to the amplifying elements is preferably formed of a variable capacitance element.

The variable capacitance element can be a MOS-type element. The MOS-type element may have an inverting layer.

Alternatively, the means of varying the state of impedance matching of the output depending on the level of the power voltage applied to the amplifying elements may be made up of an inverter which receives the power voltage and a varicap diode which has application of the output of the inverter.

For the mobile communication apparatus, the amplifying elements are preferably insulated-gate field-effect transistors.

In this case, the amplifying elements can be insulated-gate field-effect transistors connected in parallel.

Brief Description of the Drawings:

Fig.1 is a block diagram showing the mobile communication apparatus of this invention; Fig.2 is a diagram showing an example of the circuit arrangement of the RF power amplifier based on a first embodiment of this invention; Fig.3 is a graph showing an example of the operation of the inverter element used in the first embodiment; Fig.4 is a graph showing an example of the capacitance vs. voltage characteristic of the varicap

diode used in the first embodiment; Fig.5 is a set of graphs showing an example of the characteristics of the RF power amplifier of the first embodiment; Fig.6 is a diagram showing an example of the circuit arrangement of the RF power amplifier based on a second embodiment of this invention; Fig.7 is a diagram showing an example of the structure of the variable capacitance element used in the second embodiment; Fig.8 is a graph showing an example of the capacitance vs. voltage characteristic of the variable capacitance element used in the second embodiment; Fig.9 is a diagram showing an example of the circuit arrangement of the RF power amplifier based on a third embodiment of this invention; Fig.10 is a diagram showing an example of the circuit arrangement of the RF power amplifier based on a fourth embodiment of this invention; Fig.11 is a diagram showing an example of the layout of the amplifying elements and their downstream parts of the fourth embodiment; Fig.12 is a diagram showing an example of the circuit arrangement of the RF power amplifier based on a fifth embodiment of this invention; Fig.13 is a diagram showing the circuit arrangement of the RF power amplifier which has been studied prior to the present invention; and Fig.14 is a set of graphs showing an example of the characteristics of the RF power amplifier shown in Fig.13.

Best Mode for Carrying Out the Invention:

The embodiments of this invention will be explained in detail with reference to the drawings. Throughout the drawings, component parts having identical functions are referred to by the same reference symbols, and detailed explanation thereof will not be repeated.

Embodiment 1:

Fig.1 is a block diagram showing in brief the arrangement of the inventive mobile communication apparatus. The mobile communication apparatus shown in this figure is a portable telephone set, i.e., so-called cellular telephone, based on the zone selection scheme (or cell selection scheme).

The mobile communication apparatus of this embodiment is made up of an antenna 51 which transmits and receives radio waves, a transmitter 20 which modulates a low-frequency signal into a high-frequency (RF) signal of a microwave band, an RF power amplifier (RFPA) 24 which amplifies an RF signal and feeds to the antenna 51, a receiver section 30 which processes an RF signal received by the antenna 51, a control section 40 which controls these functional sections, and a battery 50 which supplies a power voltage Vdd and a reference voltage GND to these functional sections.

The transmitter 20 includes a microphone 21, a base band unit (BBU) 22 having functions of encoding and modulation, and a mixer 23. The transmitter 20 implements the digital encoding and modulation process for the signal coming from the microphone

21 or a console (CONS) 44, and thereafter converts the signal into an RF signal of a prescribed microwave band. The resulting RF signal is amplified by the RF power amplifier 24 and fed to the antenna 51 by way of an antenna duplexer (DUP) 52.

The receiver section 30 includes a low-noise amplifier (LNA) 31, a mixer 32, an intermediate frequency (IF) amplifier 33, a detector (DET) 34, a demodulator (DEM) 35, a D/A converter 36, a low-frequency (LF) amplifier 37, and a speaker 38. The receiver section 30 amplifies the RF signal coming from the antenna 51 through the antenna duplexer 52, and thereafter implements the detection and demodulation process thereby to reproduce the signal.

The control section 40 includes a local oscillator (OSC) 41, a received signal strength indicator (RSSI) 42, a control unit (CNTU) 43, a console 44 having a display and operational functions, an A/D converter 45, and D/A converters 46 and 47. The control section 40 implements selection of a base station based on the received signal strength and control of the output power of the RF power amplifier and the gain of the received signal.

Fig.2 is a diagram showing an example of the circuit arrangement of the RF power amplifier based on this embodiment. As shown in Fig.2, the RF power amplifier is made up of an input matching circuit 1, an inter-stage matching circuit 2, an output matching circuit 3, a drive circuit 4, and other parts. In Fig.2,

indicated by Pin is the input power, Vapc is the output power control voltage, Vdd is the power voltage, and Pout is the output power. An amplifying element T1 is supplied with a gate bias voltage which is produced by dividing the output power control voltage Vapc with resistors R1 and R2. The amplifying element T1 is also supplied on its drain with the power voltage Vdd through a strip line SL1.

In the output matching circuit 3, component parts identical to those of the circuit of Fig.13 which has been studied prior to the present invention are referred to by the same symbols. Specifically, the output matching circuit 3 is formed of fixed capacitors C2 (e.g.,7 pF), C3 (e.g.,1 pF), C4 (e.g,18 pF) and C10 (e.g,100 pF), and a varicap diode Cd. The output matching circuit 3 adjusts the matching state between the amplifying element T1 and the output terminal depending on the power voltage Vdd. Specifically, an inverter circuit formed of an inverter element T10 receives the power voltage Vdd to release a voltage Vd which varies inversely to the power voltage Vdd, with the voltage Vd being applied to the varicap Cd so as to adjust its capacitance.

The relation between the operation of inverter circuit and the capacitance value of varicap Cd will be explained by using Fig.3 and Fig.4. The inverter element T10 is an n-channel field effect transistor (FET) having its threshold voltage slightly lower than 3.0 V (e.g., around 2.7 V), and it has drain

current Id vs. drain voltage Vd d.c. characteristics at gate voltages Vg of 3.0 V and 3.5 V as shown in Fig.3. In Fig.3, the solid line passing through point A is the load line at a power voltage Vdd of 3.5 V, while the dashed line passing through point B is the load line at a power voltage Vdd of 3.0 V. The load lines have their slope determined from the value of a load resistor R10. The resistor R10 is 2 kΩ in this embodiment. As shown in Fig.3, the inverter element T10 has a drain voltage Vd of about 0.5 V at a power voltage Vdd of 3.5 V, i.e., at a gete voltage Vg of 3.5 V, and it is about 2 V at a power voltage Vdd of 3.0 V.

Namely, the drain voltage Vd of the inverter element T10 varies in the range from 0.5 V to 2 V in response to the variation of the power voltage Vdd in the range from 3.5 V to 3.0 V. At the same time, the varicap Cd has its capacitance Cx varying in the range from 9 pF to 6 pF approximately in response to the variation of drain voltage Vd from 0.5 V to 2 V as shown in Fig.4. In consequence, the matching (tuning) state of the output matching circuit 3 of Fig.2 is adjusted.

Fig.5 shows the resulting operational characteristics of the RF power amplifier. The figure shows by graph (A) the relation between the output power Pout and the efficiency η at the usual power voltage Vdd of 3.5 V, and shows by graph (B) the relation between the power voltage Vdd and the output power Pout. The inverter element T10 has a gate voltage Vg of 3.5

V at the usual power voltage Vdd of 3.5 V, and accordingly the drain voltage Vd is 0.5 V as revealed by the graph of Fig.3. Accordingly, the varicap Cd has a capacitance Cx of about 9 pF as revealed by the graph of Fig.4. Since the d.c. bias current blocking capacitor C10 is about 100 pF in this embodiment, the capacitance of the capacitor C10 and varicap Cd in serial connection is about 8 pF, which is the larger capacitance. This is the case of tuning with a larger capacitance, and the output matching circuit 3 is rendered the tuning of efficiency priority.

In regard to the operational characteristics of the RF power amplifier, the output power Pout is 3.6 W (target performance) and the efficiency η is 49% (point P2) at the power voltage Vdd of 3.5 V as revealed by graph (A) of Fig.5. If the power voltage Vdd falls to 3.0 V due to used-up power of the battery, the inverter element T10 has its gate voltage Vg also falling to 3.0 V, and the drain voltage Vd of the inverter element T10 applied to the varicap Cd becomes 2 V as revealed by the graph of Fig.3. Accordingly, the capacitance Cx of the varicap Cd decreases along the characteristic curve of Fig.4 to 6 pF approximately, which is the smaller capacitance. The output matching circuit 3 turns in its tuning state to the output priority, delivering the output power (point P11) which is relevant to the power voltage Vdd of 3.0 V on the dashed characteristic line on graph (B) of Fig.14. Namely, the output

power Pout of the RF power amplifier becomes 3 W (point P11) of the target performance as shown by the dashed line on graph (B) of Fig.5.

According to the operational characteristics of the RF power amplifier of this embodiment, the efficiency η is improved by about 4% from 45% (point P1) to 49% (point P2) at the power voltage Vdd of 3.5 V as revealed by graph (A) of Fig.5, while retaining the output power Pout of 3 W at the power voltage Vdd of 3.0 V as shown by the solid line P1-P11 on graph (B) of Fig.5, as compared with the operational characteristics of the RF power amplifier which has been studied prior to the present invention as shown by the dashed line on graph (B) of Fig.5 (this characteristic line is the same as the dashed line P1-P11 on graph (B) of Fig.14).

Embodiment 2:

Fig.6 is a schematic circuit diagram of the RF power amplifier based on the second embodiment of this invention. As shown in Fig.6, the RF power amplifier is made up of an input matching circuit 1, an inter-stage matching circuit 2, an output matching circuit 3, a drive circuit 4, and other parts, as in the case of the first embodiment. This embodiment differs from the preceding first embodiment in that the inverter element T10, resistor R10, capacitor C10 and varicap Cd of the output matching circuit 3 shown in Fig.2 are replaced with a variable capacitance element 11. Accordingly, the output matching

circuit 3 of this embodiment is formed of a strip line SL2, fixed capacitors C2, C3 and C4 and a variable capacitance element 11, and the matching state between the amplifying element T1 and the output terminal Pout is adjusted by the variation of capacitance of the variable capacitance element 11 depending on the power voltage Vdd. The variable capacitance element 11 and the capacitors C2 and C3 may have their positions interchanged in performing the adjustment of matching state.

An example of the structure and an example of the capacitance vs. voltage characteristic of the variable capacitance element 11 will be explained by using Fig.7 and Fig.8. The variable capacitance element 11 can be fabricated by the same process as of the amplifying element T1 of the RF power amplifier, in which a p-type epitaxial (p-epi) layer 71 is formed on a high-concentration p^{++}-type substrate 70, an n-type layer 72 is formed in the p-epi layer 71, and a high-concentration n^{+}-type layer 73 is formed in it to make ohmic contact with an electrode 74, thereby completing a MOS-type element. The variable capacitance element 11 functions by utilization of the input capacitance of the MOS-type element. The n^{+}-type layer 73 may be replaced with a high-concentration p^{+}-type layer, with the n-type layer 72 being rendered such an impurity concentration that a surface inverting layer is created by application of the power voltage Vdd.

The MOS-type element can have its input capacitance

adjusted to some extent generally based on the thickness of the oxide film (SiO_2) 75 or the concentration of ion implantation of the n-type layer 72. Specifically, the voltage dependency of the capacitance Cy required is about 6 pF at a power (terminal) voltage Vdd of 3 V and about 8 pF at a terminal voltage Vdd of 3.5 V as shown by the solid curve on the graph of Fig.8. The variable capacitance element 11 of this embodiment has its capacitance Cy saturated at about 5.5 pF in the terminal voltage Vdd range below 3 V and saturated at about 8.5 pF in the terminal voltage Vdd range above 3.5 V. However, the variable capacitance element 11 may vary much greater without any problem, provided that its characteristic is along the dashed line of Fig.8 in the terminal voltage Vdd range from 3.0 V to 3.5 V.

The RF power amplifier of this embodiment has the same operational characteristics as those of the preceding first embodiment, and it can have a higher efficiency as compared with the RF power amplifier shown in Fig.13. In addition, the RF power amplifier of this embodiment operates to adjust the variable capacitance element 11 directly by following the power voltage Vdd without increasing the circuit scale and power consumption, and it is advantageous in having no need of circuit alteration.

Embodiment 3:

Fig.9 is a schematic circuit diagram of the RF power amplifier based on the third embodiment of this invention. The

RF power amplifier of this embodiment differs from the that of the preceding second embodiment in that a fixed capacitor C5 is connected in parallel to the variable capacitance element 11 in the output matching circuit 3. This arrangement is advantageous in allowing the variable capacitance element 11 to be smaller in capacitance and size. Another advantage is that even in case there is a disparity of the center value of variation range of the capacitance of the variable capacitance element 11 attributable to the fabrication process, it can be dealt by the fixed capacitor C5.

Embodiment 4:

Fig.10 is a schematic circuit diagram of the RF power amplifier based on the fourth embodiment of this invention. As shown in Fig.10, the RF power amplifier of this embodiment is made up of an input matching circuit (not shown), an inter-stage matching circuit 2, an output matching circuit 3, a drive circuit (not shown), and other parts, as in the cases of the preceding first through third embodiments. In Fig.10, the bias voltage to be applied to amplifying elements T2 and T3 is produced by dividing the output power control voltage Vapc with resistors R1 and R2. The amplifying elements T2 and T3 are supplied on their drains with the power voltage Vdd through strip lines SL1 and SL2. The output matching circuit 3 is formed of a strip line SL2, fixed capacitors C6, C7 and C4, and a variable capacitance element 13. Based on this arrangement,

the matching state between the amplifying elements T2 and T3 and the output terminal Pout is adjusted depending on the power voltage Vdd.

The RF power amplifier of this embodiment differs from that of the preceding second embodiment in that it employs a parallel connection of amplifying elements T2 and T3 which are half in size, i.e., half in gate width W, relative to the amplifying element T1 of the second embodiment, and the amplifying elements T2 and T3 are rendered the input/output impedance matching by means of the strip lines SL1 and SL2, capacitors C11, C12, C21 and C22, and resistors R3 and R4.

The variable capacitance element 13 has the capacitance vs. voltage characteristic as shown in Fig.8, and it can be the MOS-type element of the second embodiment or a parallel connection of the fixed capacitor C5 and variable capacitance element 11 of the third embodiment. The variable capacitance element 13 has the same value of variation range as the variable capacitance element 11 of the second embodiment, although the capacitance value itself is different by the amount of the additional matching capacitors C21 and C22 at the outputs of the amplifying elements T2 and T3. Similarly, the fixed capacitors C6 and C7 are different in capacitance value from the capacitors C2 and C3 of the second embodiment due to the presence of the additional capacitors C21 and C22.

The RF power amplifier of this embodiment does not much

differ in operation and characteristics and has the same output power Pout as compared with the preceding ones, while it further gains the efficiency owing to the reduction of gate width W of the MOS transistors.

Fig.11 shows an example of the layout of the component parts located on the downstream side of the amplifying elements T2 and T3 of the circuit arrangement shown in Fig.10. The RF power amplifier is designed to be a module, in which chip parts including the capacitors C4, C6, C7, C21 and C22 and resistor R4, semiconductor chips including the amplifying elements T2 and T3, and variable capacitance element 13 are planted on a dielectric substrate 10 of ceramics, on which are formed the strip lines SL1, SL2 and SL21 of conductor such as copper.

Embodiment 5:

Fig.12 is a schematic circuit diagram of the RF power amplifier based on the fifth embodiment of this invention. As shown in Fig.12, the RF power amplifier of this embodiment is made up of an input matching circuit (not shown), an inter-stage matching circuit 2, an output matching circuit 3, a drive circuit (not shown), and other parts, as in the case of the preceding fourth embodiment. In Fig.12, a bias voltage is produced by dividing the output power control voltage Vapc with resistors R1 and R2, and applied to amplifying elements T2 and T3 through a resistor R5. The amplifying elements T2 and T3 are supplied on their drains with the power voltage Vdd through

strip lines SL3 and SL4. The amplifying elements T2 and T3 are a parallel connection of transistors which are half in size, i.e., half in gate width W, relative to the amplifying element T1 of the second embodiment, as in the case of the fourth embodiment. The output matching circuit 3 is formed of a strip line SL2, fixed capacitors C16, C17 and C4 and a variable capacitance element 14, and the matching state between the amplifying elements T2 and T3 and the output terminal Pout is adjusted depending on the power voltage Vdd.

The RF power amplifier of this embodiment differs from that of the preceding fourth embodiment in that the amplifying elements T2 and T3 have their input signals treated to be out of phase by 180° from each other by means of strip lines SL12 and SL13 and capacitors C13, C14 and C15, and have their output signals treated to be out of phase by 180° from each other by means of strip lines SL22 and SL23 and capacitors C23, C24 and C25. The variable capacitance element 14 has the capacitance vs. voltage characteristic as shown in Fig.8, and it can be the MOS-type element of the second embodiment or a parallel connection of the fixed capacitor C5 and variable capacitance element 11 of the third embodiment. The variable capacitance element 14 has the same value of variation range as the variable capacitance element 11 of the second embodiment, although the capacitance value itself is different by the amount of the additional phase-adjusting and matching capacitors C23, C24 and

C25 at the outputs of the amplifying elements T2 and T3. Similarly, the fixed capacitors C16 and C17 are different in capacitance value from the capacitors C2 and C3 of the second embodiment due to the presence of the additional capacitors C23, C24 and C25.

Based on this arrangement, when the amplifying element T2 receives an input signal on the gate, the amplifying element T3 receives the input signal which is different in phase by 180° , and these elements T2 and T3 turn on and off alternately. On the other hand, the amplifying elements T2 and T3 have their amplified outputs treated to differ in phase by 180° , and consequently the resulting output signals are in-phase with each other. Accordingly, the output power is the same as the case of parallel operation of the amplifying elements T2 and T3 of the fourth embodiment. Nevertheless, the heat dissipation is halved in this embodiment, since the amplifying elements T2 and T3 do not turn on simultaneously. The MOS transistors have their on-state resistance kept smaller, resulting favorably in a smaller thermal loss and a greater output. The amplifying elements T2 and T3 used in the RF power amplifier of this embodiment have the smaller gate width W as in the case of the fourth embodiment, and the further enhancement of power efficiency is achieved.

Although the preferred embodiments of the present invention have been explained, the present invention is not

confined to these embodiments, but various design alterations are obviously possible within the scope of the invention.

Industrial Applicability:

In the inventive mobile communication apparatus having an antenna which transmits and receives radio waves, an RF power amplifier which amplifies a power-modulated RF signal and feeds to the antenna, a receiver section which processes an RF signal received by the antenna, a control section which controls these functional sections, and a battery which supplies a power voltage to these functional sections, the RF power amplifier is made up of amplifying elements of multiple stages which amplify the RF signal, an input matching circuit which implements impedance matching for the input, an inter-stage matching circuit which implements impedance matching between the amplifying elements, and an output matching circuit which has means of varying the state of impedance matching of the output depending on the level of the power voltage which is applied to the amplifying elements. Consequently, the RF power amplifier can be lower in power consumption and higher in efficiency. This high efficiency technique will be able to make mobile communication apparatus more compact.

Claims:

1. (Amendment) A mobile communication apparatus having an antenna which transmits and receives radio waves, an RF power amplifier which amplifies a power-modulated RF signal and feeds the amplified signal to said antenna, a receiver section which processes an RF signal received by said antenna, a control section which controls these functional sections, and a battery which supplies a power voltage to these functional sections, said RF power amplifier comprising amplifying elements of multiple stages which amplify the RF signal, an input matching circuit which implements impedance matching for the input, an inter-stage matching circuit which implements impedance matching between said amplifying elements, and an output matching circuit which has means of varying the state of impedance matching of the output in proportion to the level of the power voltage which is applied to said amplifying elements.

2. (Amendment) A mobile communication apparatus according to claim 1, wherein said means of varying the state of impedance matching of the output in proportion to the level of the power voltage comprises a variable capacitance element.

3. A mobile communication apparatus according to claim 2, wherein said variable capacitance element comprises a MOS-type element.

4. A mobile communication apparatus according to claim 3, wherein said MOS-type element has a surface inverting layer.

5. (Amendment) A mobile communication apparatus according to claim 1, wherein said means of varying the state of impedance matching of the output in proportion to the level of the power voltage is formed of an inverter which receives the power voltage and a varicap diode which has application of the output of said inverter.

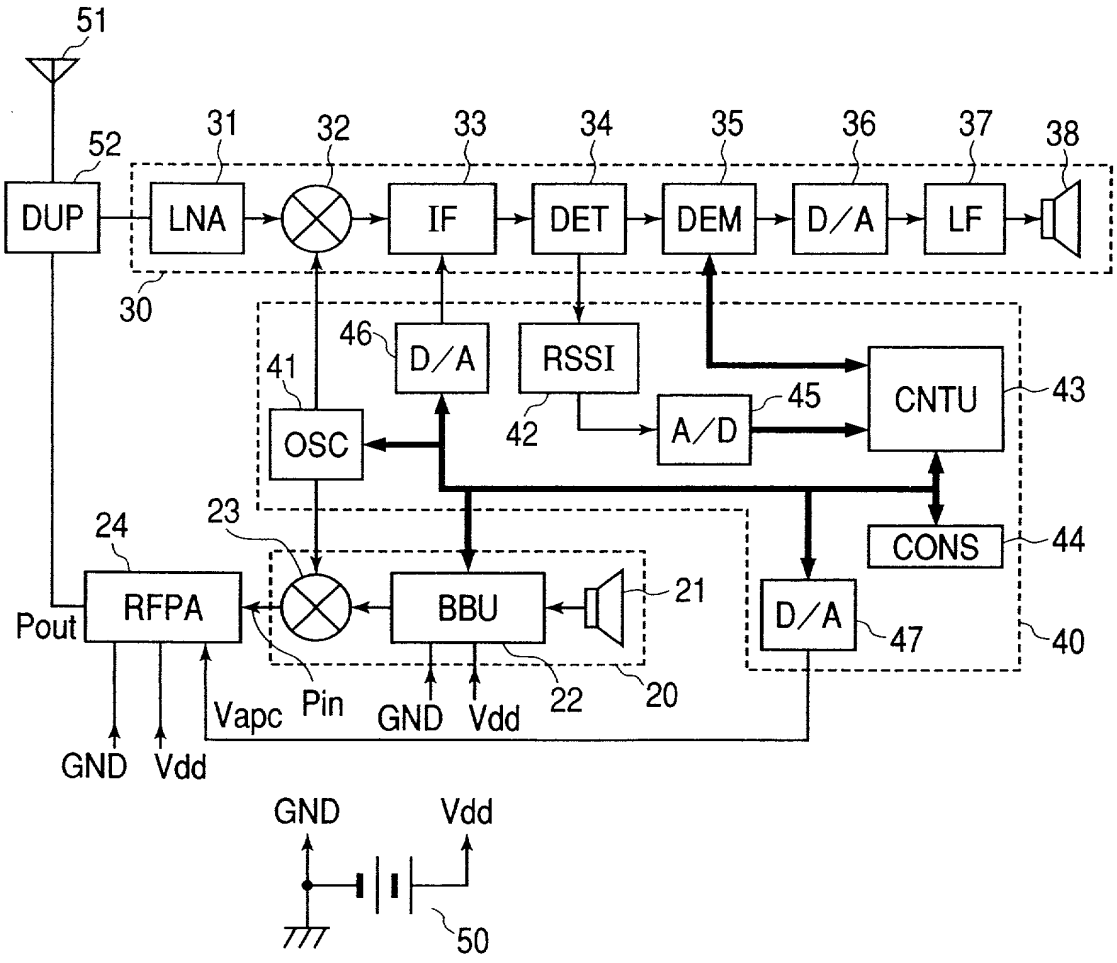
6. A mobile communication apparatus according to any of claim 1 through claim 5, wherein said amplifying element comprises an insulated-gate field-effect transistor.

7. A mobile communication apparatus according to any of claim 1 through claim 5, wherein said amplifying element comprises insulated-gate field-effect transistors connected in parallel.

Abstract:

The RF power amplifier used in the conventional mobile communication apparatus needs to have its output matching circuit adjusted by making much account of the output power at a lower power voltage. Therefore, it is problematic in that the output power is excessive at the normal power voltage, resulting in a degraded power efficiency. For overcoming this prior art deficiency of mobile communication apparatus having an antenna, RF power amplifier, receiver section, control section, and battery, the RF power amplifier is designed to include amplifying elements of multiple stages which amplify the RF signal, input matching circuit, inter-stage matching circuit, and output matching circuit having means of varying the state of impedance matching of the output depending on the level of the power voltage applied to the amplifying elements. Consequently, the RF power amplifier can be smaller in power consumption (higher in efficiency), and mobile communication apparatus can be made smaller in power consumption and in size and weight.

FIG. 1


51
52
31
32
33
34
35
36
37
38
DUP
LNA
IF
DET
DEM
D/A
LF
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46
D/A
RSSI
41
OSC
42
A/D
45
CNTU
43
CONS
44
24
23
RFPA
BBU
21
D/A
47
40
Pout
Vapc
Pin
GND
Vdd
22
20
GND
Vdd
GND
Vdd
50

FIG. 2

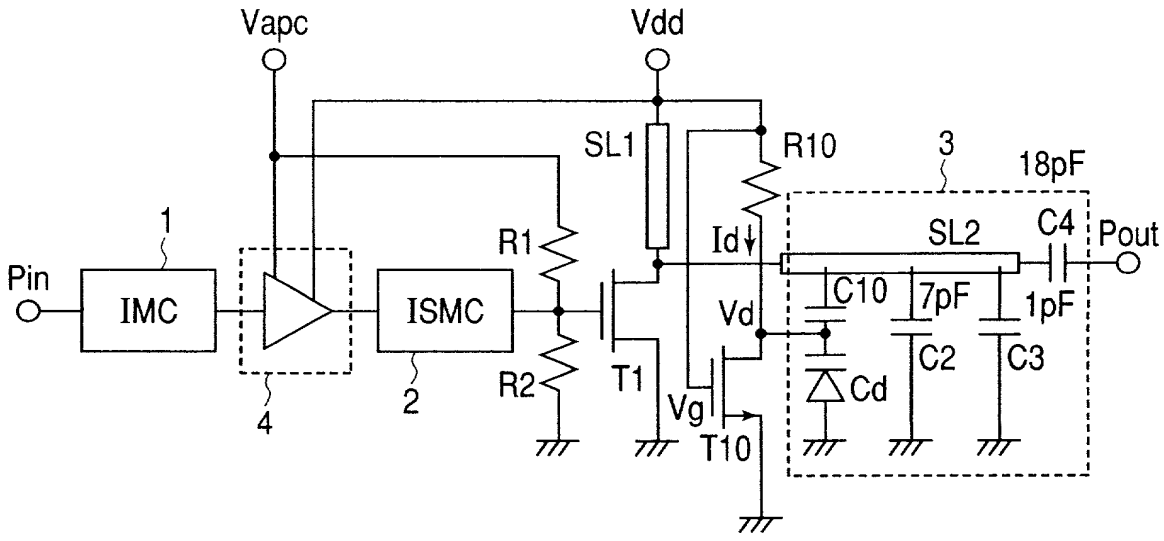

Vapc
Vdd
SL1
R10
3
18pF
1
R1
Id
SL2
C4
Pout
Pin
IMC
ISMC
C10
7pF
1pF
Vd
C2
C3
Cd
R2
T1
Vg
T10
4
2

FIG. 3

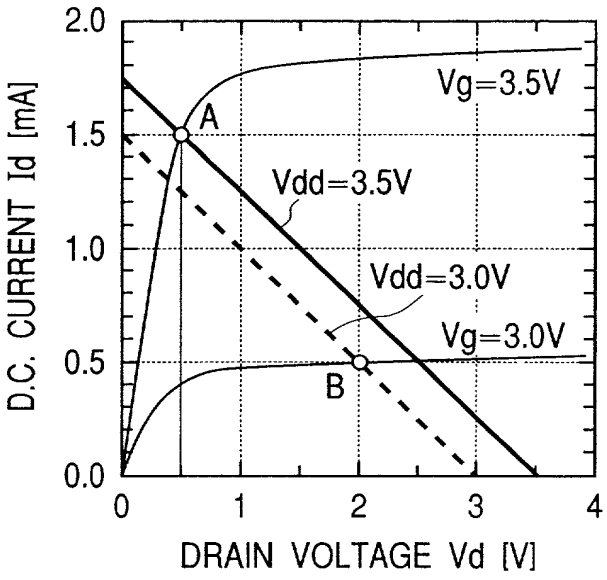

2.0
1.5
1.0
0.5
0.0
D.C. CURRENT Id [mA]
Vg=3.5V
A
Vdd=3.5V
Vdd=3.0V
Vg=3.0V
B
0
1
2
3
4
DRAIN VOLTAGE Vd [V]

FIG. 4

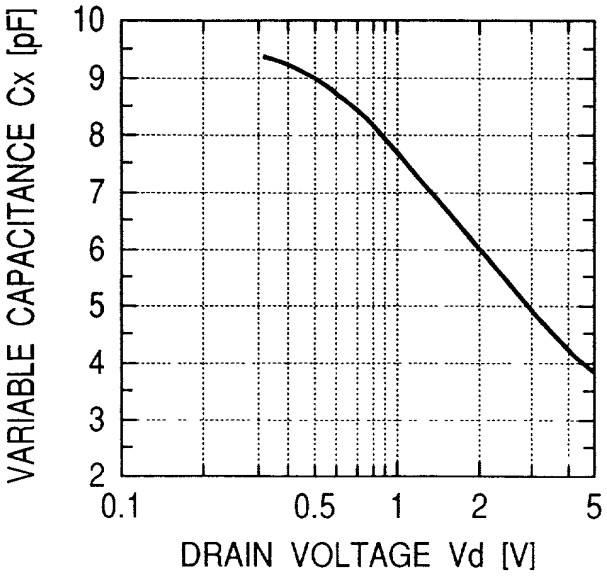

10
9
8
7
6
5
4
3
2
VARIABLE CAPACITANCE Cx [pF]
0.1
0.5
1
2
5
DRAIN VOLTAGE Vd [V]

FIG. 5(A)

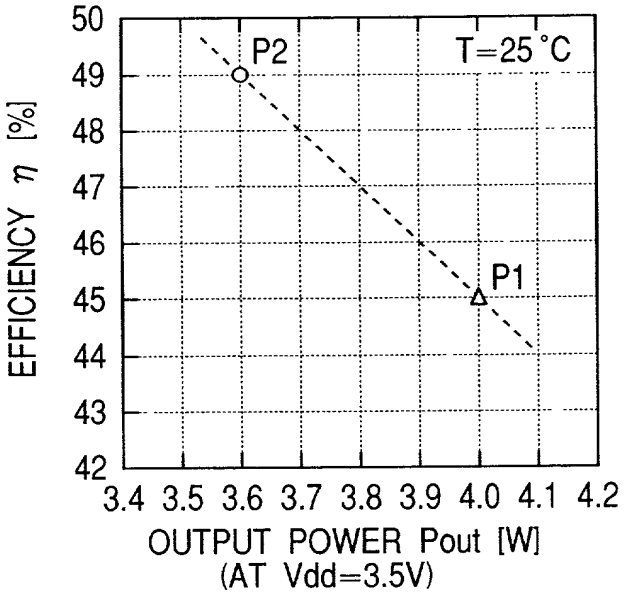

50
49
48
47
46
45
44
43
42
EFFICIENCY η [%]
P2
T=25°C
P1
3.4 3.5 3.6 3.7 3.8 3.9 4.0 4.1 4.2
OUTPUT POWER Pout [W]
(AT Vdd=3.5V)

FIG. 5(B)

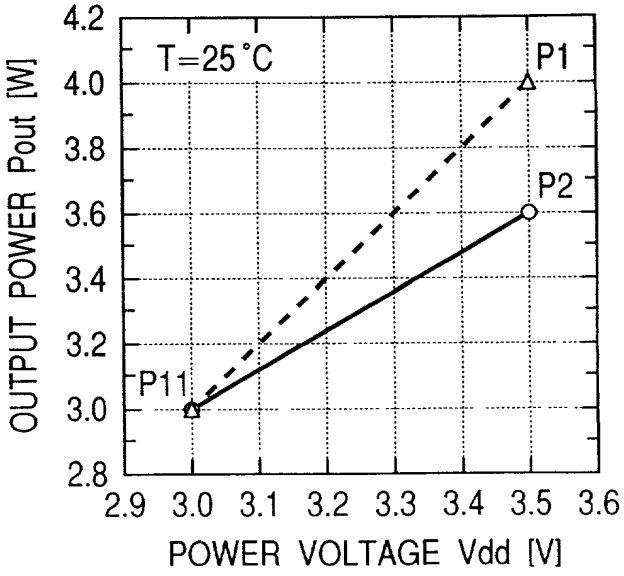

4.2
4.0
3.8
3.6
3.4
3.2
3.0
2.8
OUTPUT POWER Pout [W]
T=25°C
P1
P2
P11
2.9 3.0 3.1 3.2 3.3 3.4 3.5 3.6
POWER VOLTAGE Vdd [V]

FIG. 6

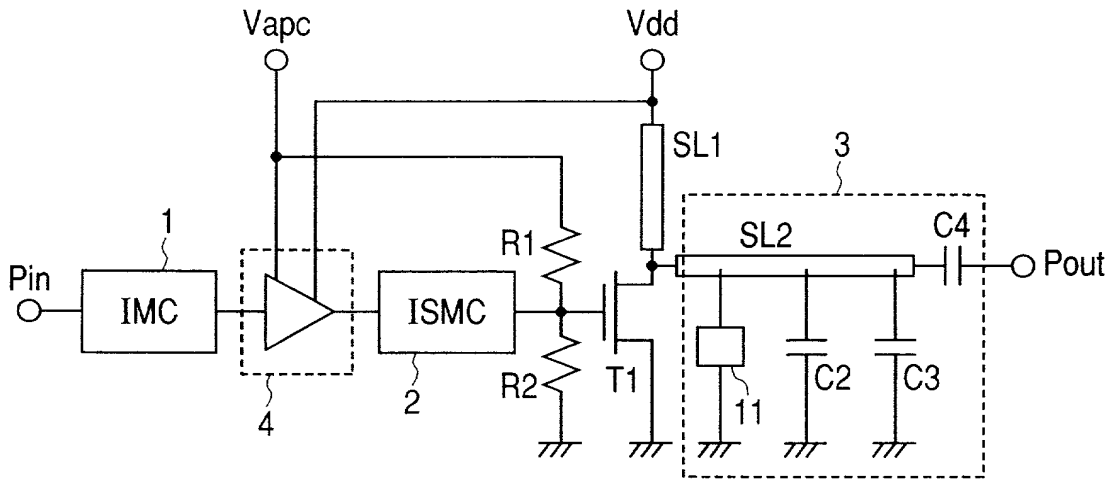


FIG. 7

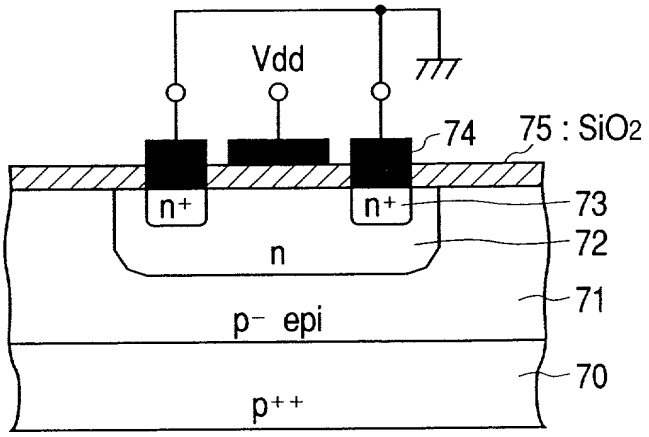

Vdd
74
75 : SiO2
n+
n+
73
72
n
71
p− epi
70
p++

FIG. 8

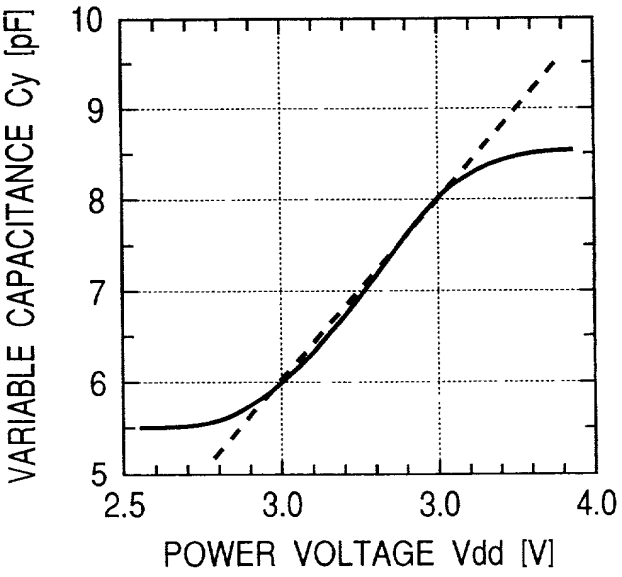

VARIABLE CAPACITANCE Cy [pF]
10
9
8
7
6
5
2.5
3.0
3.0
4.0
POWER VOLTAGE Vdd [V]

FIG. 9

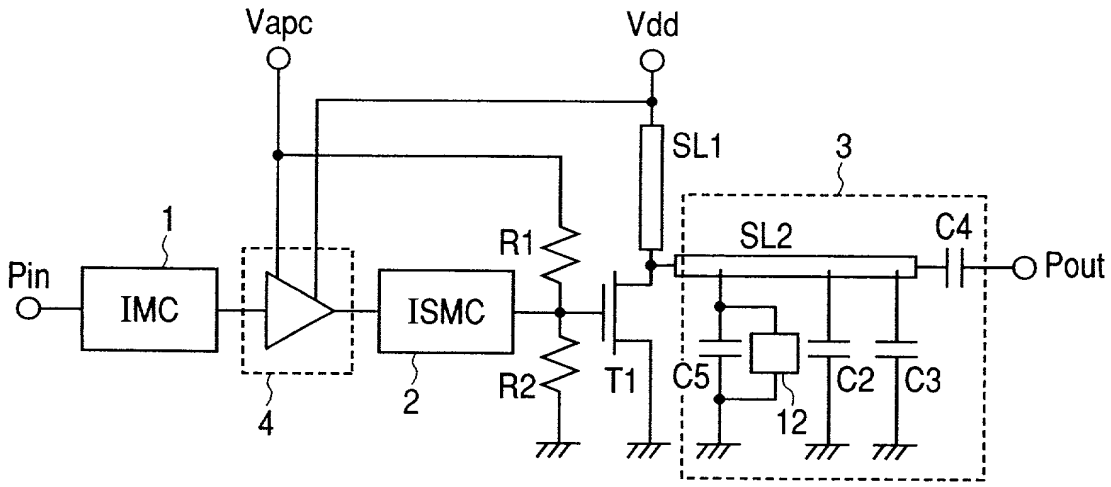


FIG. 10

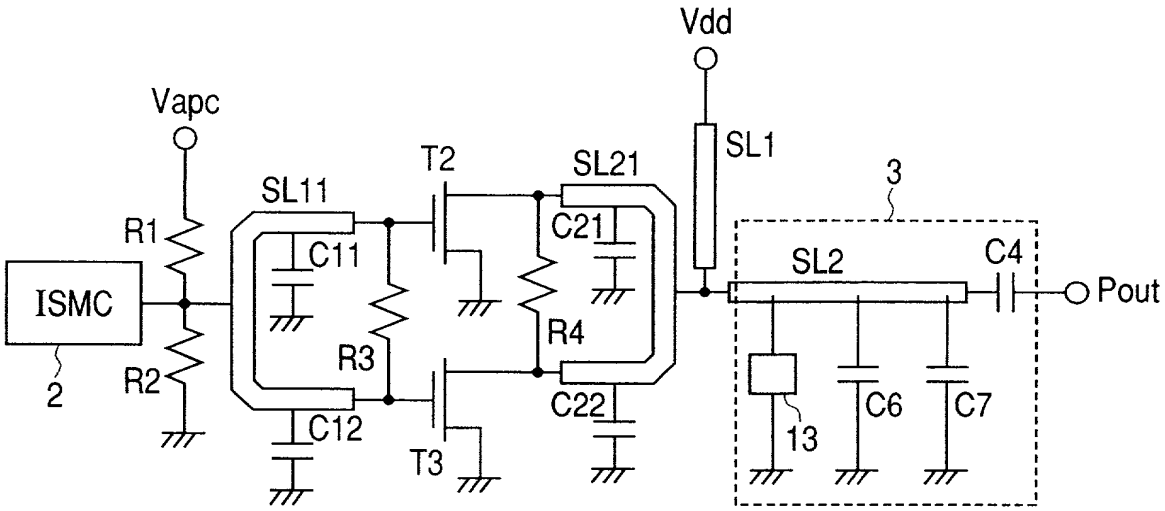

Vdd
Vapc
SL1
T2
SL21
SL11
3
R1
C21
C11
SL2
C4
ISMC
Pout
R4
R3
2
R2
C22
C6
C7
C12
13
T3

FIG. 11

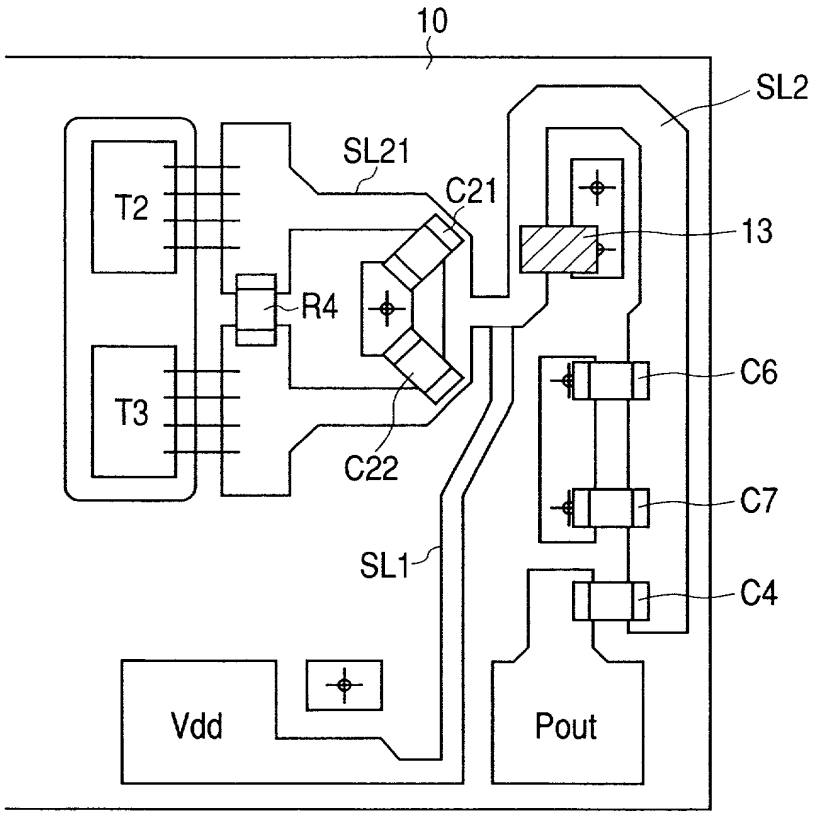


FIG. 12

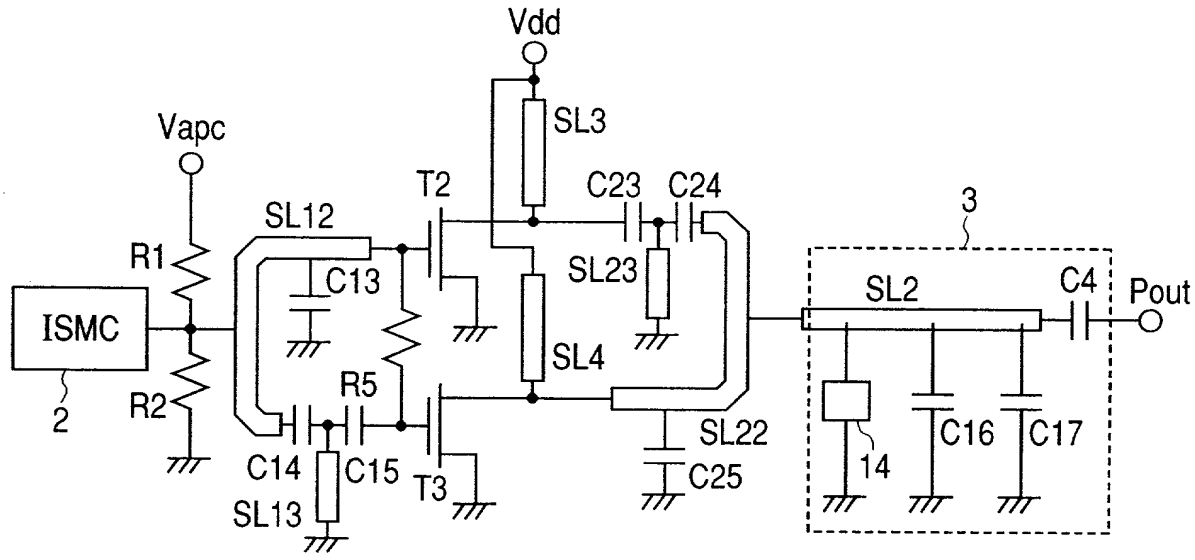

Vdd
SL3
Vapc
T2
C23
C24
3
SL12
R1
C13
SL23
SL2
C4
Pout
ISMC
SL4
R5
R2
SL22
C16
C17
2
C14
C15
T3
C25
14
SL13

FIG. 13

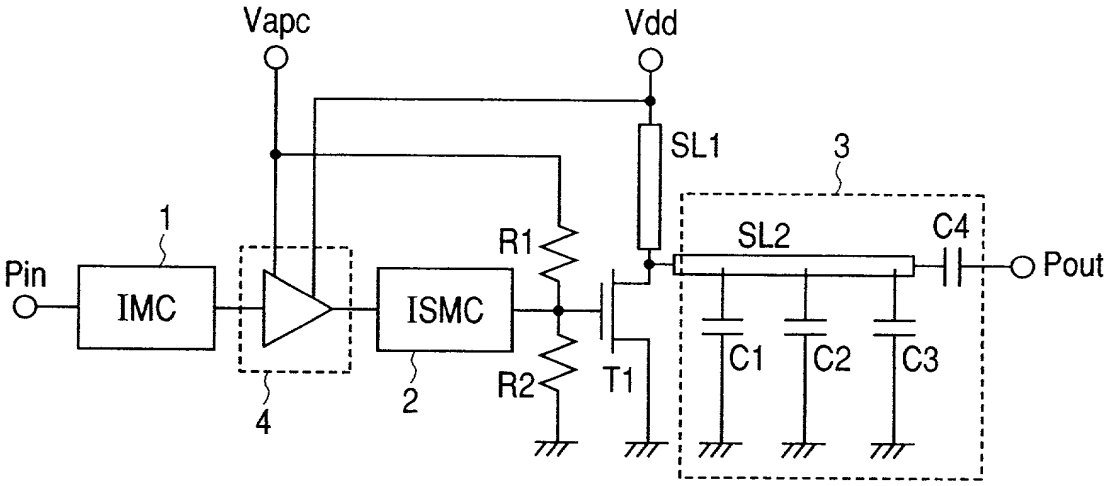


FIG. 14(A)

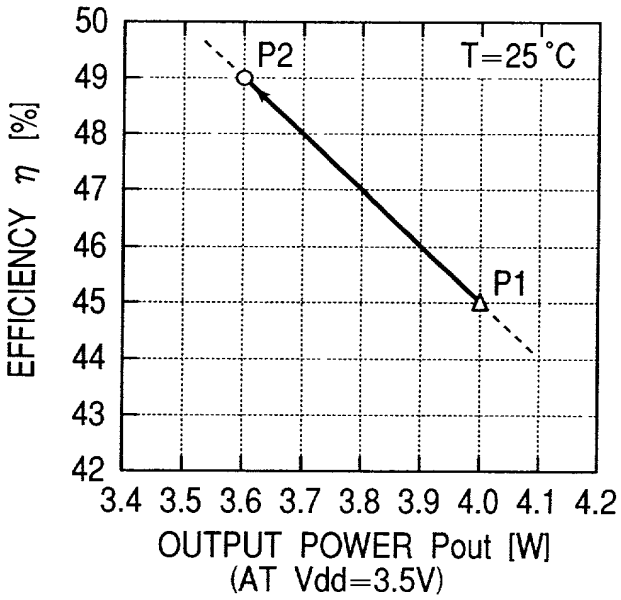
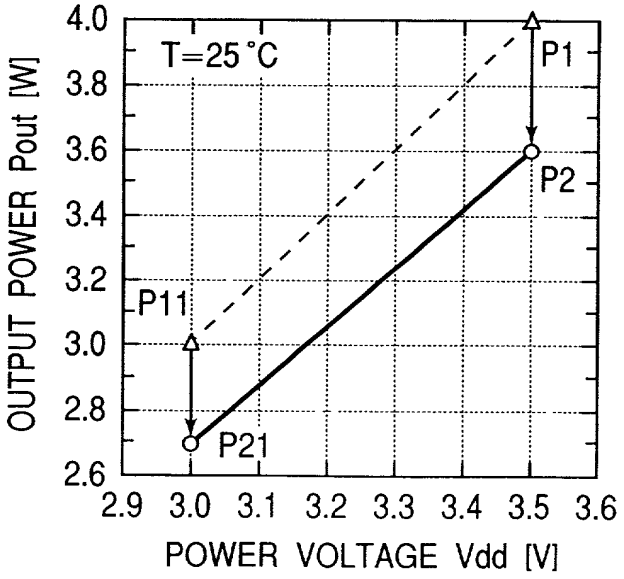


FIG. 14(B)



XA-9484
PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Yoshikuni MATSUNAGA et al.

Intl. Appln. No.: PCT/JP98/05921

Intl. Filing Date: 25 December 1998

For: MOBILE COMMUNICATION UNIT

* * *

CHANGE OF CORRESPONDENCE ADDRESS

Assistant Commissioner for Patents
Washington, D.C. 20231

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Effective immediately, please address all further correspondence in the above-identified application to:

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Respectfully submitted,

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June 18, 2001

PTO/SB/106(8-96)
Approved for use through 9/30/98. OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

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(該当する場合) _____に訂正されました。

☒ was filed on 25/December/1998
as United States Application Number or
PCT International Application Number
PCT/JP98/05921 and was amended on
_____ (if applicable).

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I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

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I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

PTO/SB/106(8-96)
Approved for use through 9/30/98. OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第３５編１１９条 (a) - (d) 項又は３６５条(b)項に基き下記の、米国以外の国の少なくとも一カ国を指定している特許協力条約３６５ (a) 項に基ずく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示している。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s) 外国での先行出願			Priority Not Claimed 優先権主張なし
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	☐

私は、第３５編米国法典１１９条 (e) 項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条 (c) に基ずく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１条５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

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(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

PTO/SB/106(8-96) (Modulated spacing)
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Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Japanese Language Declaration
(日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）	I POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number) Nelson H. Shapiro, Reg. No. 17,095, Mitchell W. Shapiro, Reg. No. 31,568, and the other practitioners associated with the Customer Number 20,230
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